



# A Single Design Environment for SDR & CR Development

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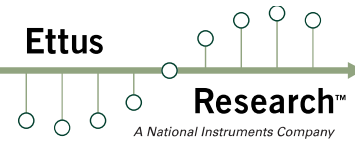
Chair of the Board of Directors, Wireless Innovation Forum



# Agenda

- Ettus Research/National Instruments Overview
- SDR & USRP Architectures
- USRP Design Flow Options
  - GNU Radio + RFNoC (Open Source)
  - LabVIEW
  - MATLAB/Simulink
- RF Network On Chip (RFNoC)
- E310 Example
- Closing Thoughts and Conclusions

# Ettus Research Overview



- Leader in Software Defined Radio (SDR) and Signals Intelligence (SIGINT)
- Maker of the Universal Software Radio Peripheral (USRP™) family
- Enables rapid development of SDR and RF systems
- Supported by a strong software ecosystem
- DC-6 GHz, MIMO capability, Embedded, USB/GigE
- Wireless Innovation Forum – 2010 Technology of the Year
- Wireless Innovation Forum – 2014 International Achievement Award
- About The Company
  - Founded in 2004
  - Located in Santa Clara, CA – Silicon Valley
  - Stand alone subsidiary of National Instruments since 2010



# National Instruments



- Leaders in Computer-Based Measurement and Automation
- Long-term Track Record of Growth and Profitability
- \$1.23B Revenue in 2015
- Invest ~16% of revenue in R&D
- > 7,000 employees; operations in 49+ countries
- Fortune's 100 Best Companies to Work For 14 Consecutive Years
- Significant investments in RF test microwave design and software defined radio



**VSAs & VSGs**



**Power Meters**



**FPGA I/O & Co-processing**



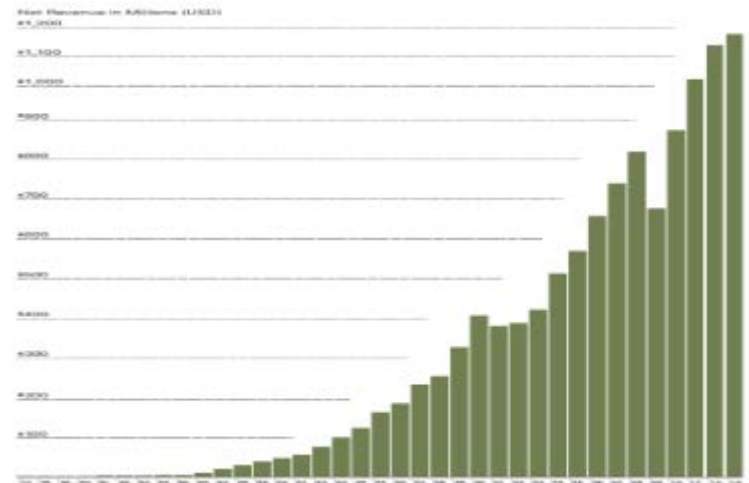
**Amplifiers & Attenuators**



**Switching**



**Software Defined Radio**



# WINNF Top 10 Innovations

1. **Innovation #1:** Techniques for Efficient Porting of Waveform Applications Between Embedded Heterogeneous Platforms
2. **Innovation #2:** Network Management of Mobile Ad-hoc Radios
3. **Innovation #3:** Receiver Performance Interference Thresholds
4. **Innovation #4:** Low Cost Wide Spectral Range RF Front-End (Multi-octave Contiguous)(Tx,Rx)
5. **Innovation #5:** Efficient Techniques to Minimize Power Amplifier Spectral Regrowth in Non-contiguous Spectral Environment
6. **Innovation #6:** Increase Communications Time on Battery Charge by an Order of Magnitude
7. **Innovation #7:** Context Aware Cognitive Radio
8. **Innovation #8:** Interference Mitigation Techniques
9. **Innovation #9:** Standardized Computer Interpretable Policy Language for Cognitive Radio
10. **Innovation #10:** Flexible Regulatory Framework for Temporary, Cooperative and Opportunistic Access

# SDR Architecture

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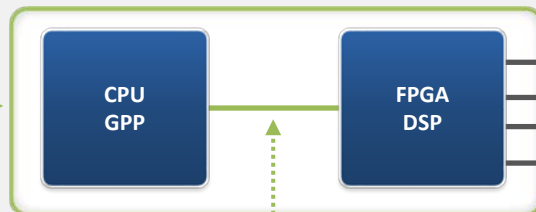
## Multi-Processor Subsystem

Real-time signal processor

- Physical Layer (PHY)
- ex FPGA, DSP

Host processor

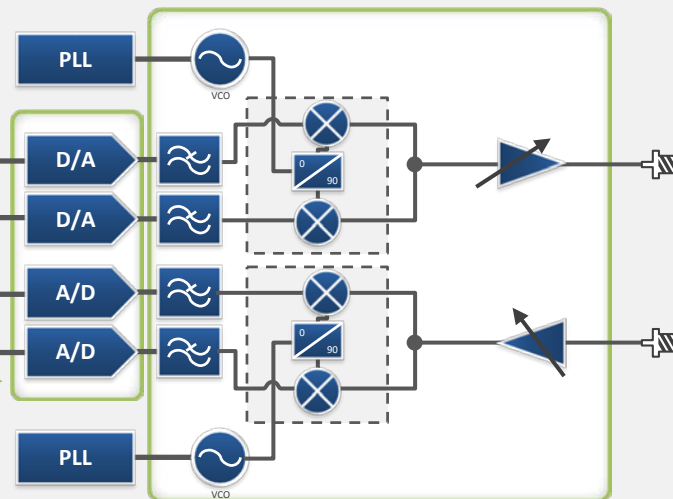
- Medium Access Control (MAC) – Rx/Tx control
- ex. Host GPP, multi-core CPU



## Host Connection

Determines Streaming Bandwidth Ex. Gigabit Ethernet, PCIe

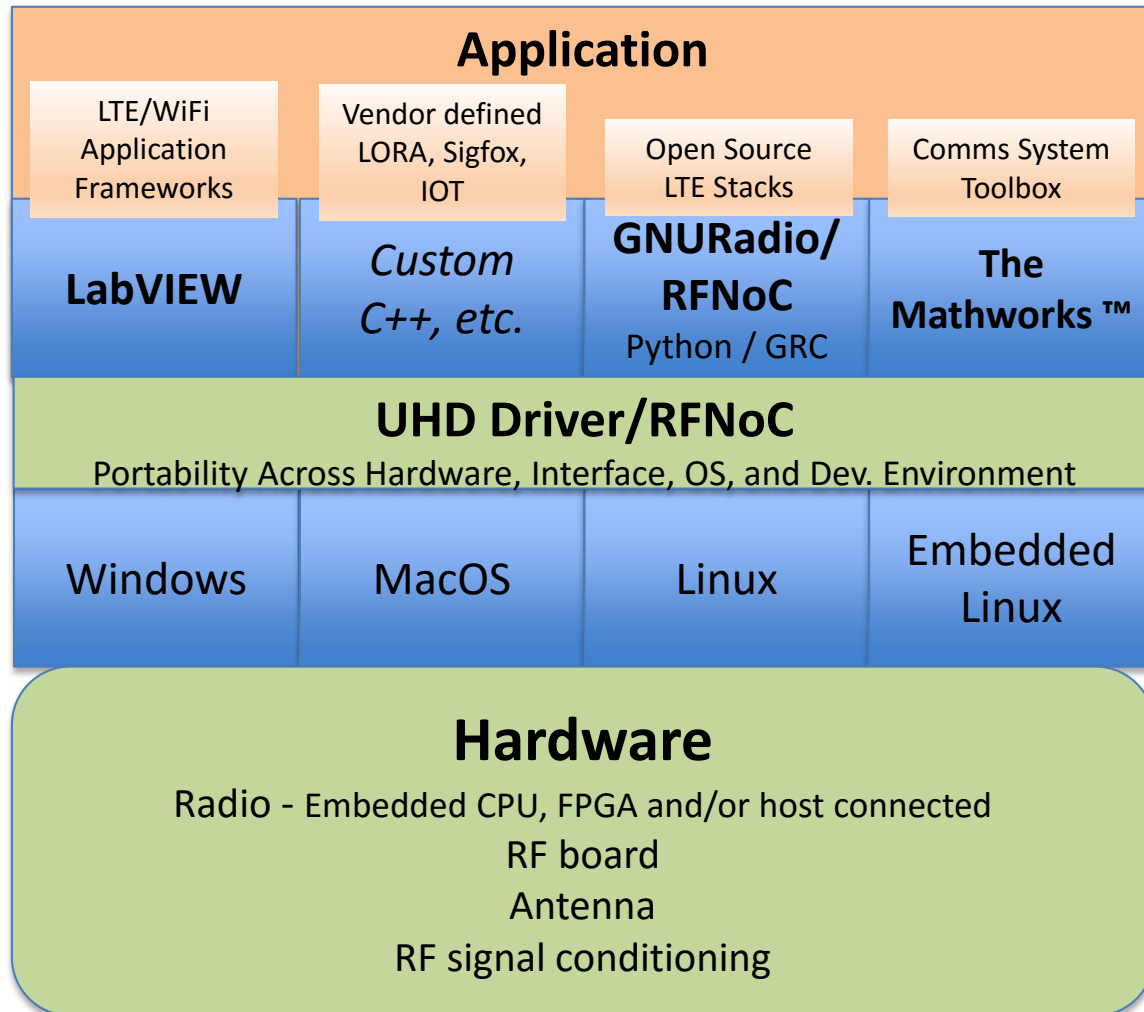
## Baseband Converters



## RF Front End

- General Purpose RF
- Dual LOs
- Contiguous Frequency Range

# USRP System Architecture



Antenna  
VERT400



RF Board  
(UBX)



USRP Radios

# USRP Unified Design Flow Options

System Model



GPP Design



FPGA Design



C/C++  
MATLAB

**NI USRP Product Family**

LabVIEW

LabVIEW  
FPGA

GNU Radio  
(GRC)

RFNoC via  
GRC

**Ettus USRP Product Family**

Embedded  
Coder

HDL Coder



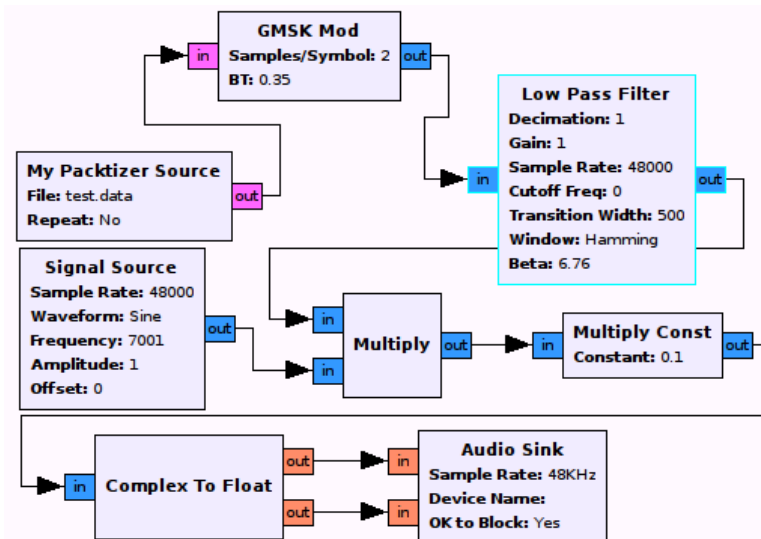
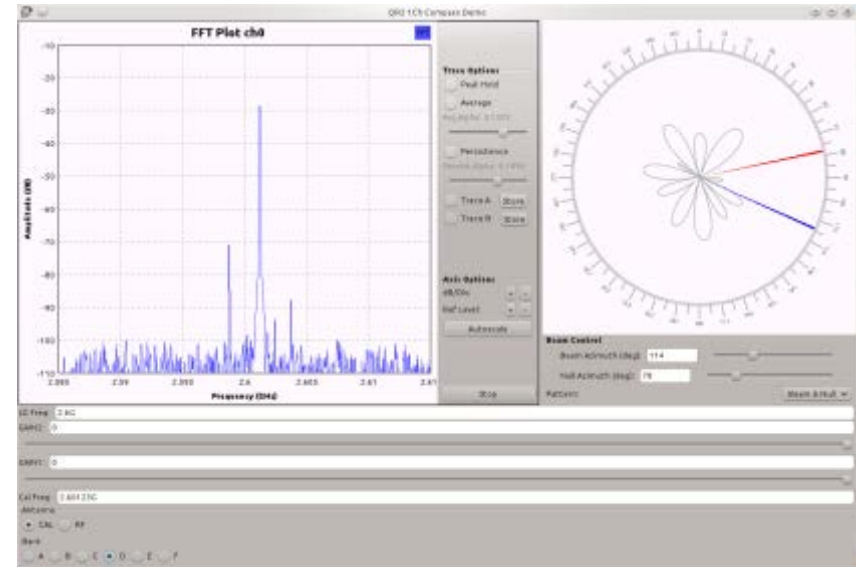
# GNU Radio Introduction

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- History
  - Experiment with ATSC Decoding in Software
  - Impetus for USRP – low cost hardware
  - Ettus Research – A Leading Contributor
- Free and Open Source
  - 1000's of users
  - Mailing List
  - [gnuradio.org](http://gnuradio.org)
  - Annual conference



# GNU Radio Design Flow

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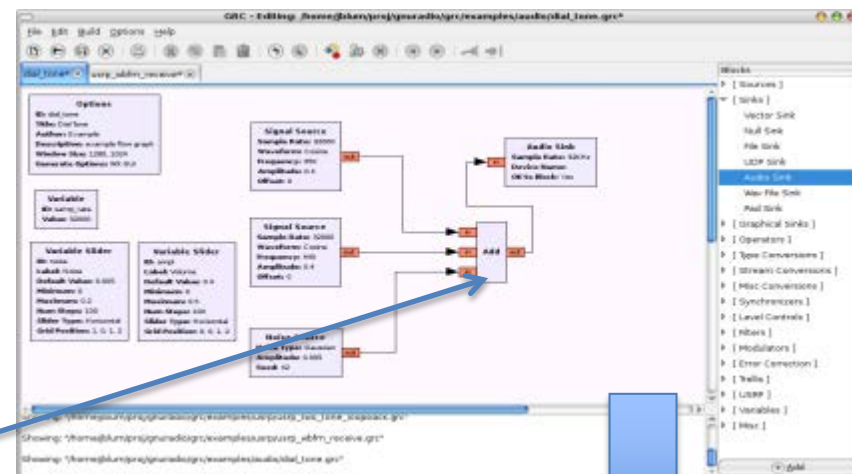
## DSP Block – C++ Work Function

```
int gr_add_ff::work(int noutput_items,
    gr_vector_const_void_star &input_items,
    gr_vector_void_star &output_items)
{
    float *out = (float *) output_items[0];
    int noi = d_vlen*noutput_items;

    memcpy(out, input_items[0], noi*sizeof(float));
    volk_32f_x2_add_32f_a(out, out, (const float*)input_items[i], noi);

    return noutput_items;
}
```

## GNU Radio Companion (optional)



## Python Flow-Graph

- Blocks
  - Large library of existing IP -> Mod/demod, filters, USRP I/O, GUI features, etc.
  - Write custom blocks – C++ or Python
- GNU Radio Companion (optional)
  - Import blocks
  - Connect blocks
  - Generate python source code for flowgraph
- Python Flow-Graph
  - Generate from GRC and/or hand-write
  - Simplifies block connectivity

```
tb = gr.top_block()

src1 = gr.sig_source_f(32000, gr.GR_SIN_WAVE, 350, .5, 0)
src2 = gr.sig_source_f(32000, gr.GR_SIN_WAVE, 440, .5, 0)

adder = gr.add_ff()

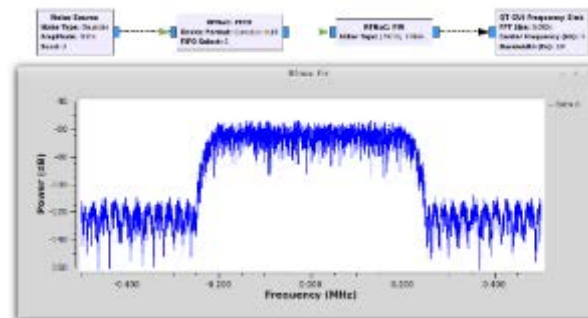
sink = audio.sink(32000)

tb.connect(src1, (adder, 0))
tb.connect(src2, (adder, 1))

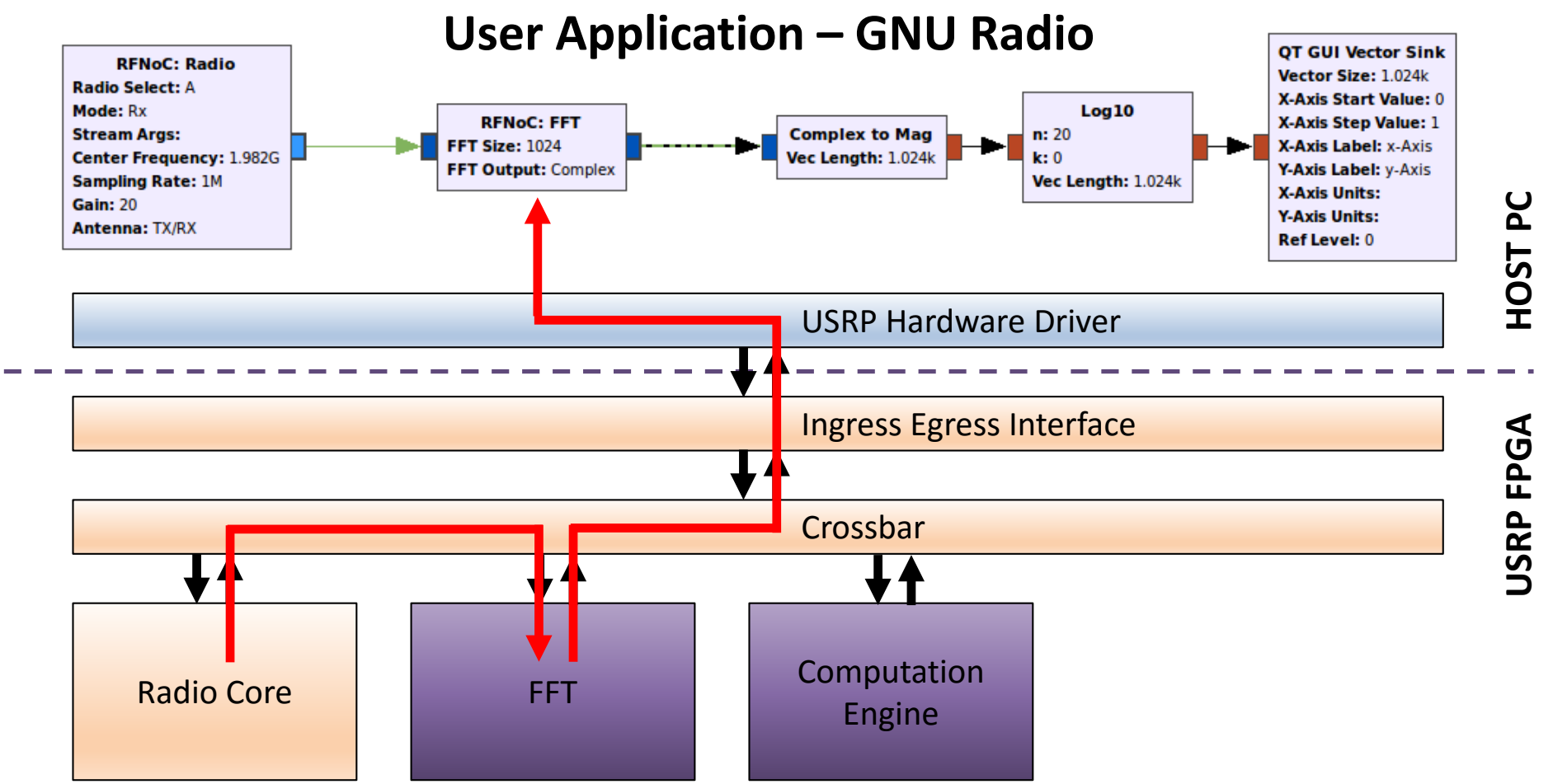
tb.connect(adder, sink)
tb.run()
```

# RFNoC: RF Network on Chip

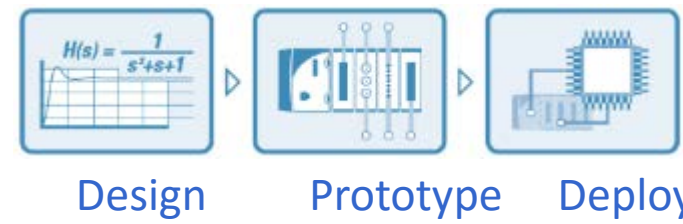
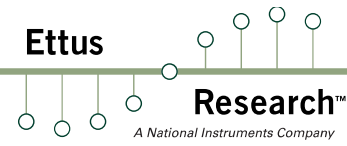
- Makes FPGA acceleration easier (especially on USRPs)
  - Software API + FPGA infrastructure
    - Handles FPGA – Host communication / dataflow
    - Provides user simple software and HDL interfaces
  - Scalable design for massive distributed processing
  - Fully supported in GNU Radio



# RFNoC Architecture



# LabVIEW Overview



A Highly Productive Graphical Development Environment for Engineers and Scientists

Hardware

**Tight H/W Integration**

**SDRs**

IP Libraries

**IP Libraries**

**Technology Abstractions**

Software

**Custom User Interfaces**

**Approaches**

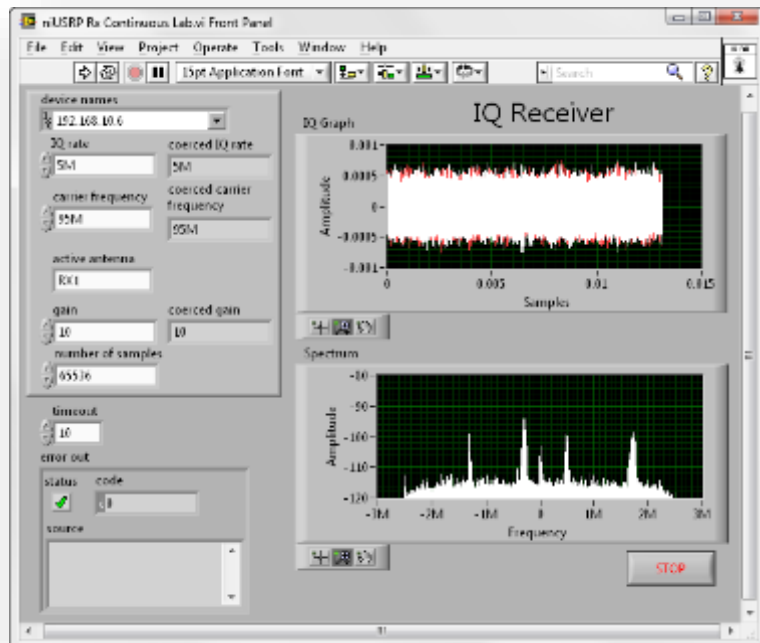


# Example: Spectrum Monitor

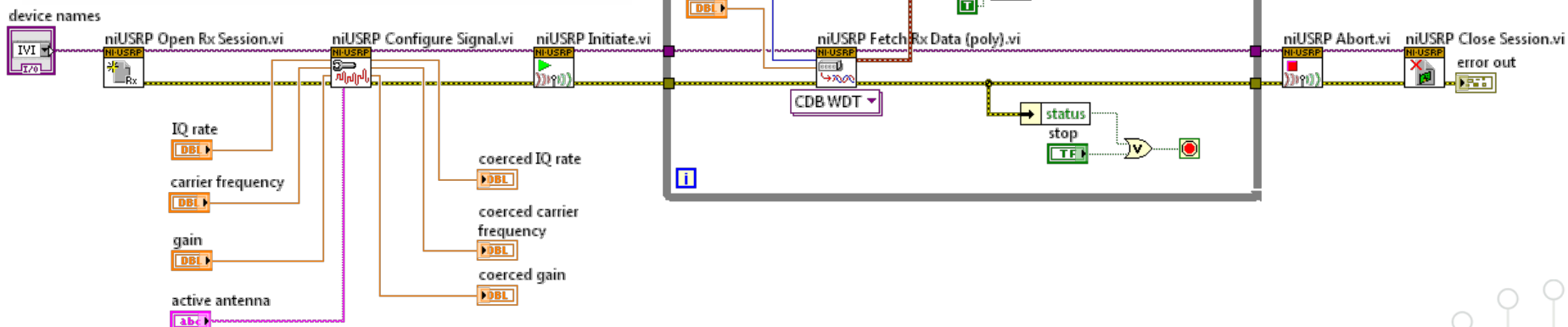
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- NI-USRP LabVIEW Driver for Windows OS
  - Modulation Toolkit & MathScript RT
- USRP2/ N200/N210 & all daughter boards
- Examples
  - 8x8 MIMO OFDM link
  - RF direction finding
  - GPS simulation
  - Spectrum monitoring
  - Record & playback



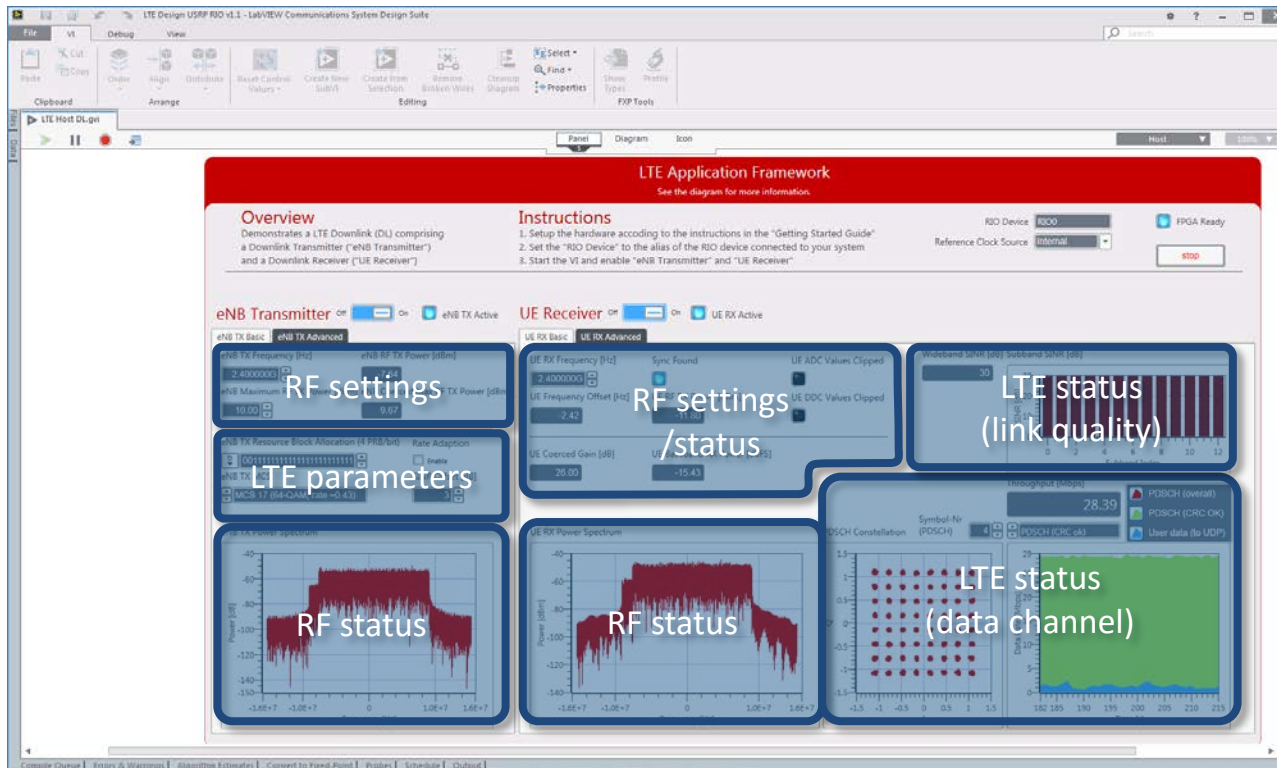
# LTE Application Framework

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## Modifiable FPGA-Based LTE eNB PHY in LabVIEW Comms





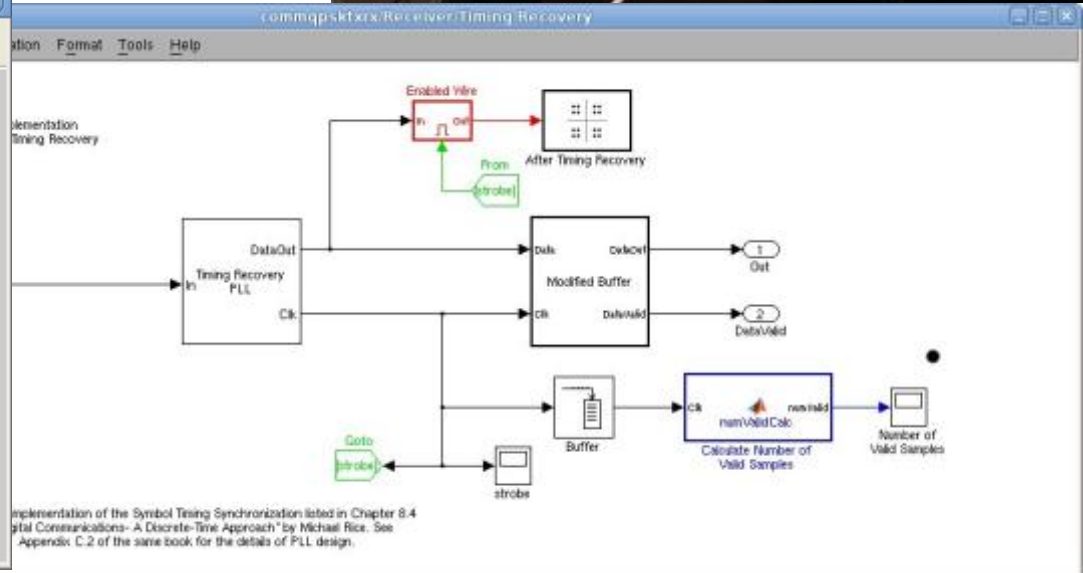
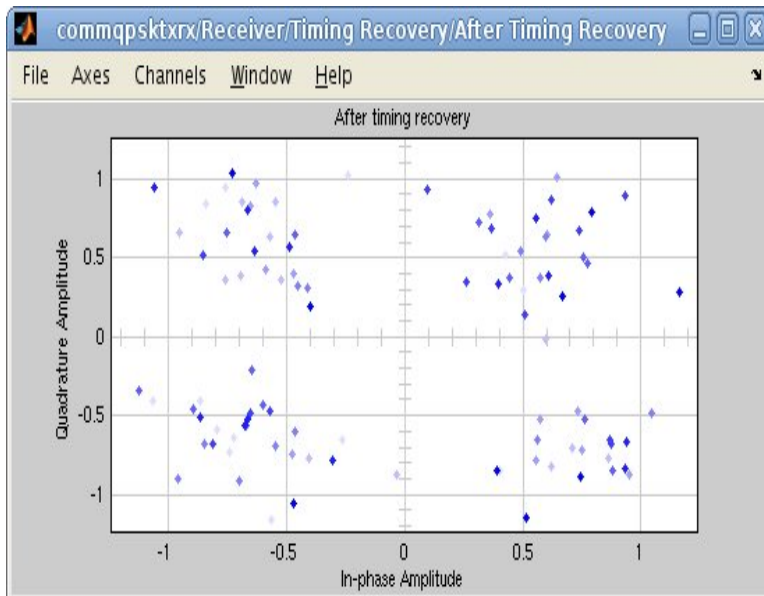
# Matlab™ and Simulink™

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- Compatible with Matlab Scripts and Simulink Models
  - Communications blockset/toolbox
- FPGA supported by HDL Coder
- USRP N210, B210, X310, E310
- Examples
  - QPSK transmitter and receiver
  - FM mono and stereo receiver
  - FRS/GMRS transmitter and receiver





# USRP E-Series Overview

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## Specs

- Frequency Range: 70MHz - 6 GHz, 10dBm power output
- Analog Devices 9361 with filter banks
- 2x2 MIMO standard configuration
- ~ 50 MHz BW / channel
- Xilinx Zynq-7020
  - ARM Dual-Core Cortex A9 @ 886 MHz
  - 1GB MB Processor RAM
  - 512 MB FPGA RAM
- 133x68x26.4 mm, 375g
- 3-9 W



## Applications

- Mobile Network research
- Network testbeds
- Small, portable, low cost spectrum monitor
- Small UAVs
- Handheld universal communicator

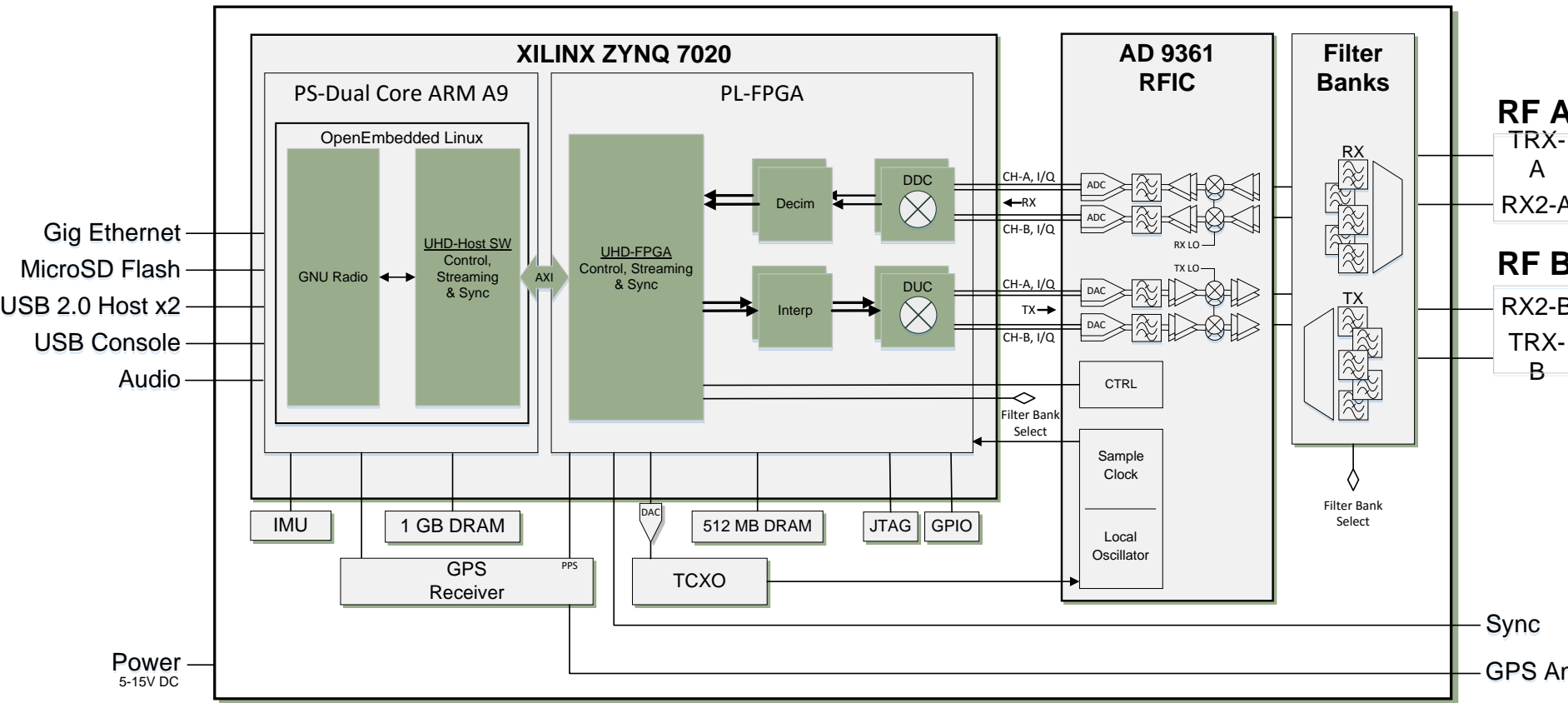
## Derivatives

- E313 - Waterproof - IP67
- E330 - 4 Rx to TDOA/DF Applications
- E312 - Battery

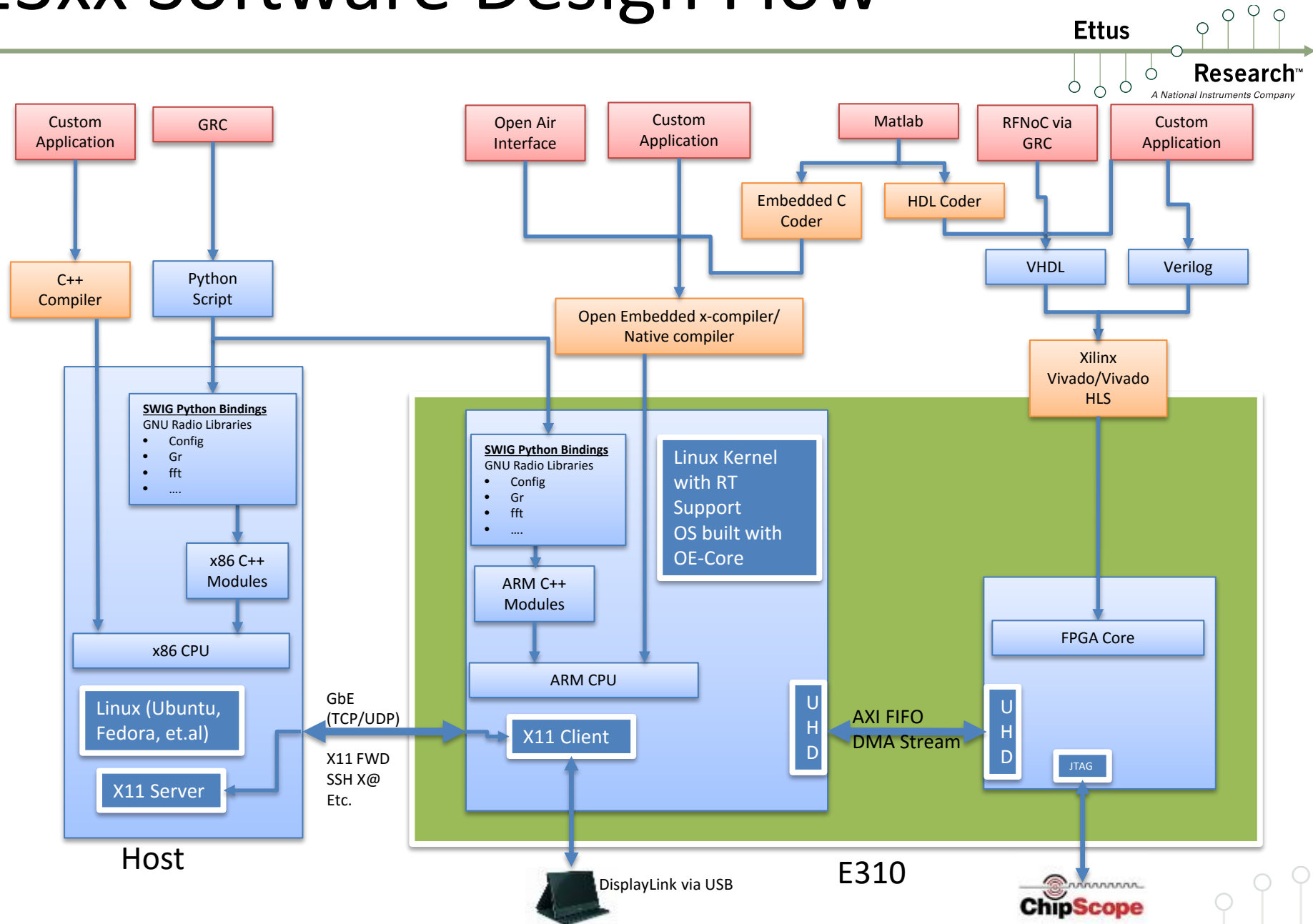
## Features

- I/O: GigE, Audio in/out, USB 2.0 Host, GPS In
- Micro SD memory card slot
- GPS Receiver

# USRP E-Series Block Diagram



# E3xx Software Design Flow



# Closing Thoughts and Conclusions



- SDR waveform design on and across heterogeneous processors is still difficult
- But there are tools that can help!
  - GNU Radio + RFNoC, LabVIEW Comms (including LabVIEW FPGA), MATLAB/Simulink + Embedded C Coder + HDL Coder
- All 3 heterogeneous development environment options are graphical-based
  - Nice, easy-to-use way to visualize the processing amongst processors
  - Still designed to take algorithms developed in code, wrap them in code, but display the system model graphically
- The USRP family of devices can support all 3 options

Thank You!

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